IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

In re Application of

Eric B. KUSHNICK

Art Unit: 2116

Application No: 09/824,898

Examiner:
Tse W. Chen

Filed: April 2, 2001

For: HIGH RESOLUTION CLOCK SIGNAL GENERATOR

REPLY BRIEF

COMMISSIONER FOR PATENTS
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Sir:

The applicant provides the following comments in reply to paragraph (10) of the Examiner's Answer.

Claims 1, 2, 4-8 and 11

The Examiner argues that Christiansen teaches a delay circuit (FIG. 10), that Hondeghem teaches a programmable sequencer (70, 84, 112) producing repetitively varying control data (116, 118), and that one of skill in the art would be motivated to use Hondeghem's sequencer to repetitively vary control data to Christiansen's delay circuit because both references relate to "signal generation" and because doing so permits Christian's delay circuit to operate with "higher

resolution." The following comments are provided in reply to the Examiner's argument.

a. Although it may be possible to configure Hondeghem's CPU 70, RAM 84 and I/O logic 112 to behave as a sequencer that produces repetitively varying control data on lines 116 and 118 in response to an input pulse sequence, Hondeghem does not teach that such is the function of CPU 70, RAM 84, and I/O logic 112. Hondeghem's specification indicates how CPU 70, RAM 84 and I/O logic circuit 112 are interconnected but does not teach anything about what they do, does not teach lines 116 and 118 convey control data that varies in a repetitive fashion in response to pulses of any particular signal, and does not teach or suggest that data on lines 116 and 118 control the delay of the stages of a two-stage delay circuit or any other kind of delay circuit. The Examiner cites Hondeghem col. 5, lines 35-36 as teaching the purpose of lines 116 and 118, but that section of Hondeghem states only that the "I/O logic circuits 112 are connected to the period frequency selector 108 and the sub-interval frequency selector 110 by means of lines 116 and 118" and provides no discussion of the function of CPU 10, RAM 8, I/O logic circuits 112, selectors 108 and 110 or the nature of signals conveyed on lines 116 and 118. Nor does Hondeghem provide any indication that these elements have anything to do with generating "sequences shown in figure 3" as the Examiner suggests. In any case, the sequences in Hondeghem's figure 3 referenced in Hondeghem col. 6, lines 45-48 are not sequences of repetitively

varying data for controlling delays as recited in claim 1; they are signal pulse sequences which Hondeghem (col. 10, lines 29-33) teaches should be used for stimulating living tissue.

b. Although the Examiner believes there would be a benefit ("higher resolution") to combining the teachings of Christiansen and Hondeghem, the Examiner's belief is insufficient support for the assertion that one of skill in the art would be motivated to do so in the absence of a showing that the cited references themselves teach or suggest such benefit. Regardless of whether Hondeghem teaches a device that repetitively varies control data, nothing in Christiansen or Hondeghem teaches or suggests that the control data input (sel) to Christiansen's delay circuit of FIG. 10 ought to vary in a repetitive manner or suggest that doing so would provide "higher resolution" or any other benefit.

c. Since every electronic device ever conceived, from transistors to supercomputers, involves some sort of "signal generation", the Examiner's assertion that one of skill in the art would be motivated to combine the teachings of Hondeghem and Christiansen in the manner suggested by the Examiner since they both "are involved in the field of signal generation" is not a convincing showing that one would be motivated to combine teachings of the two references. While both references talk about electronic devices, which of course involve "signal generation," they relate to distinctly different areas of technology. Christiansen's paper relates to a circuit for extracting a clock signal from a data signal received by an

integrated circuit while Hondeghem's patent relates to equipment for generating signals that Hondeghem teaches should be used for stimulating biological tissues (see col. 1, lines 77-11).

d. The Examiner incorrectly argues that one of skill in the art would be motivated to vary the control data input (sel) to the two stages of Christiansen' delay circuit of FIG. 10 because doing so would allow it to operate with "higher resolution". Increasing timing resolution is not the benefit provided by varying the first and second control data as recited in claim 1. Although the applicant's control data varies repetitively and Christiansen's control data is held constant, the timing resolution of Christensen's delay circuit of FIG. 10 is exactly the same as that of the applicant's circuit illustrated by FIGs. 5, 7 and 8, assuming that each has the same number N of elements in its first delay stage, and the same number N-1 of elements in its second delay stage. Repetitively varying the control data inputs (sel) to each stage of Christiansen's delay would not improve resolution; as discussed below, it would lower resolution. Thus a desire to "improve resolution" would not motivate one of skill in the art to vary the control data in Christiansen's circuit.

e. Repetitively varying the first and second control data input to the applicant's first and second delay stages (54 and 56 of FIG. 5) is beneficial because it allows the circuit to produce an output CLOCK' signal having a period that differs from the period Tp of the input ROSC signal, without affecting the

resolution or accuracy of output signal edge timing. However one of skill in the art would not be motivated to vary the control data inputs (sel) of Christiansen's delay first and second delay stages of FIG. 10 in order to change the period of the circuit output signal because doing so would lower the resolution of Christiansen's delay circuit and likely render the timing of edges of the output signals (out) unpredictable. The second stage of Christiansen's delay circuit forms a feedback loop including a delay line formed by a set of gates, along with a phase detector and loop filter for controlling the delay of each gate of the delay line by controlling its supply voltage to bring the stage and delay line input signal into phase. The feedback loop holds the delay of each stage to exactly Tp/N or Tp/(N-1) where Tp is the period of the first stage output signal which acts as the second stage input signal. The remarkably high resolution and accuracy with which Christiansen's delay circuit controls timing of edges of the output signal hinges on the fact that each delay element of the first stage has a delay held precisely to Tp/N and that each delay element of the second stage has a delay held precisely to Tp/(N-1) such that the ratio of first and second stage element delays is N/(N+1). This precise ratio between the delays of elements of the two stages creates a vernier effect permitting very high timing resolution using a relatively small number of gates whose delays are actually larger than the resolution of the delay circuit. If one were to repetitively vary the control data input to Christiansen's first

delay stage so that it produced an input signal to the second stage having a period other than a constant Tp, then the delay of each delay element of the second stage would be driven to something other than Tp/(N-1), thereby destroying the precise delay ratio needed to provide the necessary vernier effect thereby lowering timing resolution. Note also that the stability of the feedback loop of the second stage requires the period Tp between edges of the output signal of the first stage, which forms the input signal to the second stage, to be constant. If the control data input to the first stage were to vary such that the period between edges of the first stage output signal is not always constant (which would be necessary in order to produce most possible output signal periods), transients in the feedback loop of Christiansen's delay circuit would result in unstable, unpredictable second stage element delays. (Though not recited in claim 1, the applicant's circuit avoids this problem by using a second stage as illustrated in FIG. 7 in which the delay of each delay element 60 is Tp/(N-1) but which, unlike element delays in Christiansen's second stage, is independent of the period of the output signal of the preceding stage.) Since repetitively varying control data (sel) inputs to the first and second stages of Christiansen's delay circuit would lower its resolution and render it unfit for its intended function of or producing a stable clock signal having predictable edge timing, one of skill in the art would not be motivated to do so.

Claims 20, 21, 23-27, 30, 34 and 35

The Examiner incorrectly argues that the minimum delay of each stage of Christiansen's delay circuit of FIG. 10 is zero. The delay provided by Christiansen's delay circuit includes the sum of delays though all gates in the signal path between the stage's input signal and the stage's output signal. From FIG. 10 we see that at least one gate is always in the signal path through each stage regardless of the choice made by the stage's output multiplexer. Thus the minimum delay through each stage will always be at least Tp/N or Tp/(N-1).

Claims 3 and 22

Claims 3 and 22 recite that at least one of the first and second delay ranges is wider than the period Tp of the input first sequence. The Examiner incorrectly characterizes Christensen as teaching a first or second delay range wider than Tp. Referring to Christiansen's FIG. 10, given the period of the input signal (in) is Tp, since the delay of each of the N gates of the first stage is Tp/N, the maximum delay is Tp when the output of the last stage is selected. The minimum first stage delay is Tp/N with the output of the first stage selected. Thus the delay range of the first stage is Tp - Tp/N, which is always less than Tp regardless of the value of N. Similarly, it can be seen that the delay range of the second stage, which has N-1 gates, is Tp - Tp/(N-1), which is also less than Tp.

In Heyne's delay circuit of FIG. 1, the delay of each gate can vary with temperature, and therefore the range of each stage can vary with temperature. That is why Heyne teaches to make the range of the delay circuit large enough to accommodate expected variations in delay range due to changes in individual gate delays resulting from temperature variations. Although the Examiner correctly cites Heyne as showing a two-stage delay circuit having a delay range selected to be wide enough to "compensate for the maximum fluctuation range due to temperature influences", the Examiner incorrectly argues that Heyne would motivate one of skill in the art to "just add an additional delay element" to expand the range of Christensen's first or second stage to be wider than Tp in order to compensate for temperature influences.

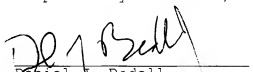
First, neither Christiansen nor Heyne teach or suggest how to increase the range of either of Christiansen's delay stages above Tp. If one were to follow the Examiner's suggestion and "just add an additional delay element" to either delay stage of Christiansen's delay circuit of FIG. 10, the feedback circuit would decrease the delay of each gate element of the stage's delay line such that the range of the stage [T- Tp/N] or [Tp - Tp/(N-1)] would still be less than Tp. The range of a stage would approach Tp as elements were added but would never rise above Tp regardless of the number N of delay elements one may add to its delay line.

Second, note that Heyne does not teach that the ranges of his delay stages should have any particular relationship to the period of their input signals which, unlike the inputs to Christensen's delay stages, need not even be periodic. Thus whatever things Heyne teaches to consider when choosing the range of a delay stage, the period of the input signal to be delayed is not one of them.

Third, and perhaps most importantly, one of skill in the art would not be motivated to increase the range of either of Christiansen's delay stages beyond Tp (however that might be done) to compensate for "temperature influences" as the Examiner suggests, because temperature has no influence at all on the delay ranges provided by Christiansen's delay stages. Although the delay of a gate does vary with its supply voltage and its temperature, each of Christiansen's delay stages of FIG. 10 includes a feedback system that adjusts the supply voltage of each gate forming its delay line so that despite any variation in gate temperature, the delay of the gate is held precisely at Tp/N or Tp/(N-1). Since temperature variation has no influence on the delay of any gate forming either of Christiansen's delay lines, temperature has no influence on the delay range of either of Christiansen's delay stages. Heyne would therefore not motivate one of skill in the art to modify either of Christensen's delay stages to provide a range wider than the period Tp of its input

signal in order to compensate for "fluctuation in delay range due to temperature influences" as argued by the Examiner.

Respectfully submitted,



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